FIRST PRELIMINARY AMENDMENT

October 20, 2000

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Drawings:

Please transfer FIGS. 1 – 2, 3B – 3D, and 4 – 13 from the file of the issued `070 patent to the reissue file.

Please amend FIGS. 3A and 3E as requested in the enclosed Request for Drawing Change.

In the Specification:

In Column 3, line 6, please replace "PG1 and PG2" with ~~[~~[PG1 and PG2] TG1 and TG2~~]~~.

In Column 4, please replace with "$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}$" with

$$[\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}]$$

$$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \times \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \times \frac{Vcc - Vt_{pd}}{Vcc - Vt_{tg}}$$

In the Claims:

Please amend the claims as follows:

1. An SRAM memory cell comprising:

[a] first and second transfer gate transistors, the first transfer gate transistor having a first source/drain connected to a bit line and the second transfer gate transistor having a first source/drain connected to a complement bit line and each transfer gate transistor having a gate connected to a word line; [and]

first and second pull-down transistors configured as a storage latch, the first pull-down transistor having a first source/drain connected to a second source/ drain of said